QUARTERLY TECHNICAL REPORT

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EVALUATION OF PULSED UV-LASER GAS PHASE DOPING FOR FABRICATION OF HIGH PERFORMANCE POLYSILICON TFTS

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I. SUMMARY

The primary purpose of this research effort is to investigate and characterize the use of Gas Immersion Laser Doping (GILD) for the fabrication of polysilicon TFTs. To achieve this goal we will be investigating the fabrication of poly-Si TFTs using both standard, industrially recognized doping and annealing processes along with and laser processing and annealing.

II. TECHNICAL REPORT

THIN FILM TRANSISTOR DEVELOPMENT

During the first quarters effort we have designed a process flow for the fabrication of simple TFTs and materials test structures useful for evaluation and comparison of laser and furnace processed polysilicon material. The processing and doping experiments are shown in Table I, all experiments are performed on LPCVD a-Si (~1000Å) deposited on thermally oxidized (1000Å) (100) 4in Si wafers.

Wafer ID	Furnace Anneal	Pattern Islands	Laser Anneal	Ion Imp Gate	GILD S/D/G	Ion Imp S/D/G	Furnace Anneal	Laser Anneal
D1-D5	x	x	x	x	x	-	-	-
D6-D10	x	x	-	x	x	-	-	-
D11-D12	x	x	x	-	-	x	x	-
D13-D15	x	x	x	-	-	x	-	x
D16-D17	x	x	-	-	-	x	x	-
D18-D20	x	x	-	-	-	x	-	x
D21-D25	x	t	-	t	-	t	-	-
D26-D29	x	-	t	-	t	-	-	-

x = process this step - = skip this step t = test wafer this step

Table I Process Variables TFT Run I

The condensed process flow, not listing cleans, etc. is listed following.

TFT Process Flow:

1. Grow 1000Å thermal oxide
2. Deposit 1000Å LPCVD a-Si at 550°C
3. Furnace recrystallization at 600°C, 20 hrs in argon
4. Pattern active device area using plasma etch
5. Laser anneal appropriate wafers

6. Deposit gate oxide, 1000Å LTO at 400°C
7. Densify gate LTO, 600°C for 20hrs in O_2
8. Deposit gate poly-Si, 3000Å LPCVD at 600°C
9. Implant gate, $1x10^{15}cm^{-2}$, phosphorus at 60 keV GILD Wafers
10. Anneal gate implant, 600°C, 1hr in argon GILD Wafers
11. Pattern gate, plasma and wet etch
12. Implant gate, source, and drain, $1x10^{15}cm^{-2}$, phosphorus at 60 keV II Wafers
13. Furnace anneal implant, 600°C, 1hr argon II Wafers
14. Strip LTO
15. Laser Anneal II and Laser Anneal Wafers
16. GILD process GILD Wafers
17. Deposit 6000Å LTO at 400°C
18. Define Contact Windows
19. Al(1%Si) metallization
20. Contact definition
21. Sinter, 400°C, 30min forming gas
22. Cover Front side wafer with Photoresist
23. Dry etch backside (remove all deposited layers)
24. Strip Photoresist
25. Electrical Test
26. Hydrogenation
27. Electrical Test

The final device cross-section is shown in Figure 1.

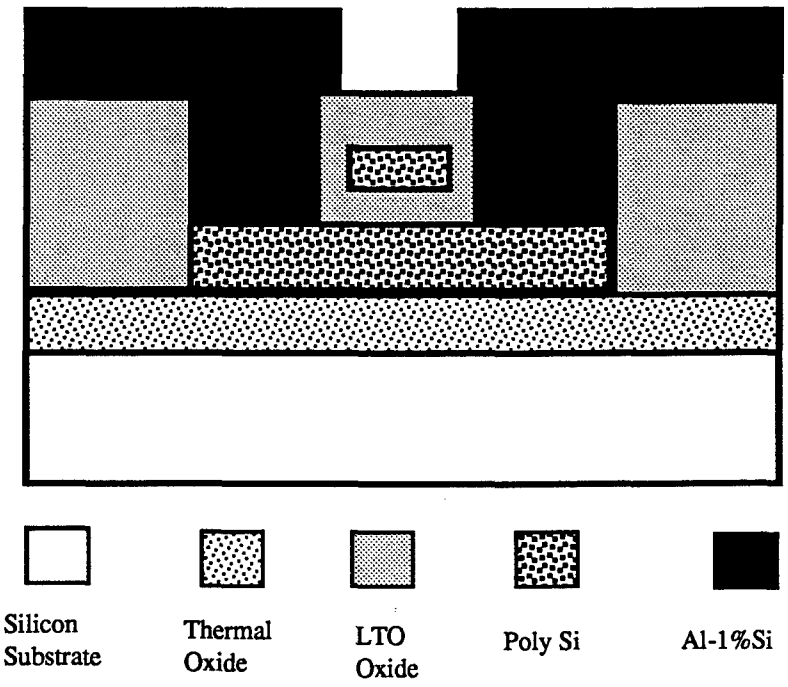

Figure 1 TFT Device Cross Section

III. FUTURE EFFORT

During the next quarters effort will consist of:

i) Begin processing Run I of the TFT process.

ii) Begin investigating the liquid phase deposition of SiO_2 at temperatures near to room temperature.